AMENDMENTS TO THE CLAIMS

1. (Currently amended) A communications system comprising:

a decision feedback equalizer adapted to reduce channel related distortion in received data, wherein the decision feedback equalizer is configured to generate[[s]] equalized data; and

a clock and data recovery circuit coupled to the decision feedback equalizer, wherein the clock and data recovery circuit is configured to generate[[s]] an extracted clock signal from the equalized data and wherein the decision feedback equalizer includes a retimer that is configured to generate[[s]] recovered equalized data from the equalized data in response to the extracted clock signal.

2. (Currently amended) The communications system of claim 1 wherein the decision feedback equalizer comprises a summer that is configured to generate[[s]] a combined signal by combining an equalized feedback signal with the received data to reduce the channel related distortion.

3. (Currently amended) The communications system of claim 2 wherein the decision feedback equalizer further comprises a slicer coupled to the summer, wherein the slicer is configured to generate[[s]] the equalized data by converting the combined signal into a binary signal and wherein the clock and data recovery circuit is configured to generate[[s]] the extracted clock signal from the binary signal.

4. (Currently amended) The communications system of claim 3 wherein the retimer comprises a flip flop coupled to the slicer and the clock and data recovery circuit and wherein the flip flop is configured to generate[[s]] the recovered equalized data from the binary signal in response to the extracted clock signal.

5. (Currently amended) The communications system of claim 3 wherein:

the clock and data recovery circuit comprises a frequency acquisition loop and a phase lock loop,

~~wherein~~ the frequency acquisition loop is configured to adjust[[s]] a frequency of the extracted clock signal to maintain a fixed relationship between a frequency of the binary signal and the frequency of the extracted clock signal, and

~~wherein~~ the phase lock loop is configured to adjust[[s]] a phase of the extracted clock signal to maintain a fixed relationship between a phase of the binary signal and the phase of the extracted clock signal.

6. (Currently amended) The communications system of claim 5 wherein the clock and data recovery circuit further comprises a frequency lock detector ~~for determining~~ configured to determine when the frequency of the extracted clock signal is fixed relative to the frequency of the binary signal.

7. (Currently amended) The communications system of claim 6 wherein:

the decision feedback equalizer further comprises a multiplier coupled to the retimer, ~~and wherein~~ the multiplier ~~applies~~ being configured to apply an equalization coefficient to the recovered equalized data to generate the equalized feedback signal, and

the decision feedback equalizer is configured to automatically iterate the equalization coefficient until the clock and data recovery circuit synchronizes with a frequency of the equalized data.

8. (Currently amended) The communications system of claim [[7]] 6 wherein:

the decision feedback equalizer further comprises a multiplier coupled to the retimer, the multiplier being configured to apply an equalization coefficient to the recovered equalized data to generate the equalized feedback signal, and

the multiplier ~~applies~~ is configured to vary the ~~a predetermined~~ equalization coefficient ~~upon startup~~ based on a level of inter-symbol interference in the received data.

9-16. (Canceled)

17. (Currently amended) A communications system comprising:

a decision feedback equalizer adapted to reduce channel related distortion in received data, the decision feedback equalizer comprising:

a summer that is configured to combine[[s]] an equalized feedback signal with the received data,

a slicer coupled to the summer, ~~wherein~~ the slicer being configured to convert[[s]] the combined signal to a binary signal,

a retimer coupled to the slicer, ~~wherein~~ the retimer being configured to generate[[s]] recovered equalized data from the binary signal in response to an extracted clock signal, and

a multipler coupled to the retimer, ~~wherein~~ the multiplier being configured to apply ~~applies~~ an equalization coefficient to the recovered equalized data to generate the equalized feedback signal, and

a clock and data recovery circuit coupled to the slicer, ~~wherein~~ the clock and data recovery circuit being configured to generate[[s]] the extracted clock signal from the binary signal.

18. (Currently amended) The communications system of claim 17 wherein:

the clock and data recovery circuit comprises a frequency acquisition loop and a phase lock loop, ~~wherein~~ the frequency acquisition loop being configured to adjust[[s]] a frequency of the extracted clock signal to maintain a fixed relationship between a frequency of the binary signal and the frequency of the extracted clock signal, and

~~wherein~~ the phase lock loop is configured to adjust[[s]] a phase of the extracted clock signal to maintain a fixed relationship between a phase of the binary signal and the phase of the extracted clock signal.

19. (Currently amended) The communications system of claim 18 wherein the clock and data recovery circuit further comprises a frequency lock detector ~~for determining~~ configured to determine when the frequency of the extracted clock signal is fixed relative to the frequency of the binary signal.

20. (Currently amended) The communications system of claim 19 wherein the multiplier ~~applies a predetermined~~ is configured to vary the equalization coefficient ~~upon start up~~ based on a bit error rate of the received data.

21. (Original) A method of reducing channel related distortion in received data comprising:

providing received data to a decision feedback equalizer;

generating, by the decision feedback equalizer, a binary signal according to the received data;

extracting a clock signal from the binary signal; and

retiming the binary signal according to the clock signal.

22. (Currently Amended) The method of claim 21 further comprising:

maintaining a fixed frequency relationship between the binary signal and the extracted clock signal by adjusting [[the]] a frequency of the extracted clock signal; and

maintaining a fixed phase relationship between the binary signal and the extracted clock signal by adjusting [[the]] a phase of the extracted clock signal.

23. (Currently amended) The method of claim 22 wherein the ~~fixed phase relationship is maintained~~ maintaining the fixed relationship includes maintaining the fixed relationship after determining that the frequency of the extracted clock signal is fixed relative to [[the]] a frequency of the binary signal.

24. (Original) The method of claim 21 further comprising applying at least one predetermined equalization coefficient to the decision feedback equalizer upon startup.

25. (Original) The method of claim 21 further comprising modifying at least one equalization coefficient to synchronize frequencies of the extracted clock signal and the binary signal.

26. (Original) The method of claim 25 further comprising adjusting at least one equalization coefficient to reduce inter-symbol interference after synchronizing the frequencies of the extracted clock signal and the binary signal.

27. (New) The communications system of claim 1, wherein the decision feedback equalizer further comprises a multiplier configured to scale the recovered equalized data by an equalization coefficient, the equalization coefficient being based on a bit error rate of the received data.

28. (New) The communications system of claim 1, wherein:

the decision feedback equalizer further comprises a multiplier coupled to the retimer, the multiplier being configured to apply an equalization coefficient to the recovered equalized data to generate the equalized feedback signal, and

the clock and data recovery circuit further comprises a frequency lock detector configured to adjust the equalization coefficient based on a frequency difference exceeding a threshold, the frequency difference being based on a frequency of a reference clock included in the clock and data recovery circuit and a frequency of a divided signal, the divided signal being generated from the extracted clock signal.